Design of low power SRAM Cell with combined effect of sleep stack and variable body bias technique

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***Abstract*: Power consumption has become major concern in Very Large Scale Integration circuit and according to International technology roadmap of semiconductors (ITRS) leakage power dissipation may dominate more of total power dissipation [1]. Sub threshold leakage power tends to increase as the leakage power increases. Variable sleepy biased keeper is compared with previously available technique like Sleep, Stack, Sleepy Stack, Sleepy Keeper, and Zigzag.**

In this paper, we design SRAM cell by combining two techniques, namely sleep stack and body biasing technique. The sleepy stack reduces leakage power, but loses its logic state during sleep mode. And body biasing technique reduces the static power consumption and maintains the logic state of the circuit. One main advantage of using variable sleepy biased keeper is, it can also use high V_{th} transistors.

Keywords: IRTS, sleepy keeper, sleepy stack, power rail, SSVVBB, SRAM, LECTOR

1. INTRODUCTION

Power consumption is one of the top concerns in VLSI circuit design, in which Complementary Metal oxide Semiconductor is a primary technology. Focus on the low power is not only because of the growing demand of the mobile applications but it has become the cutting edge for the latest technology. To solve this problem many researchers have proposed several methods from circuit level to the architectural level and above.

Power consumption of CMOS consists of static power and dynamic power. Dynamic power is consumed when the transistor switch from ON to OFF and vice versa. Static power is consumed regardless of switching. Sub threshold leakage current becomes prime concern as it increases exponentially with the threshold voltage.

Static SRAMs are extensively used in modern processors due to their large storage density. In order to meet the low dynamic power consumption and standby power, VDD of SRAM is lowered. In order to ensure the adequate run time in read and write operation, VDD is maintained little higher than the minimum supply voltage. This paper analyzes low leakage in SRAM cell along with speed improvement.

2. RELATED WORK

Power Gating: Power gating is the technique of disconnecting the component temporarily that is not in use [2]. And this technique uses the sleep transistor to cut off power from the supply rails. Typically low leakage PMOS transistors are used as header switches to shut-off power supply. Footer NMOS devices are also used to control power supply to the circuit.

Sleep Transistor: This is a state destructive technique, which cuts off power rails or ground by using sleep transistors [3]. It uses PMOS sleep transistors between power supply rails and pull up network and NMOS sleep transistors between ground and pull down network. This technique dramatically reduces the leakage power by cutting of the power supply rails with area and delay overhead. During sleep mode, it loses its state as pull up and pull down network is floating. Thus it increases the wake up time of the transistor.

Sleepy Stack: This technique combines the sleep and stack approaches [4]. It divides the transistors into halves and then the sleep transistors are added in parallel to the divided transistors. During sleep mode, sleep transistors are turned off, thus suppressing the leakage current while saving the state. So delay is decreased during the active mode.

MTCMOS: Auto back gated Multi threshold voltage (ABC-MTCMOS) uses reverse bias to reduce the leakage power [5]. This is a state preserving technique, which preserves the logic state of the circuit. RBB reduces the leakage power by increasing the threshold voltage without losing the state of the circuit.

Sleepy Keeper: It is the improved version of sleep approach [6]. In this technique, an additional high V_t NMOS transistor is added in parallel with sleep PMOS transistor and high V_t NMOS is added in parallel with sleep PMOS. In sleep mode, sleep transistors are is cut off state. So, when sleep signal is asserted, the high V_t NMOS transistor connected in parallel with the sleep PMOS transistor is the only source of V_{dd} to the pull up network and the high V_t PMOS transistor connected in parallel with the sleep NMOS transistor provides the path to connect the pull down network with the ground. Thus the major advantage of this approach is it reduces the leakage power thereby maintaining the logic state of the circuit.

Zigzag approach: Zigzag approach reduces the area overhead caused by the additional sleep transistor in sleep approach [7]. By placing the alternate sleep transistor this overhead can be reduced by selecting the particular preselected input vector. In sleep mode, input of logic is '0' and each logic input reverses its state and the output is 1. Thus, the zigzag approach uses few sleep transistors than the sleep logic.

Input Vector Control (IVC): Leakage power value has strong dependence on the input combinations. This technique uses the input vector to control the leakage power [8]. The input vector which gives the low leakage is chosen by the automation technique and applied to the circuit under sleep mode.

GALEOR - Gated Leakage Transistor: GALEOR reduces the leakage current flowing through the circuits [9]. In this technique, two gated leakage transistors are inserted between NMOS and PMOS circuitry of the existing circuit such that gates of the extra inserted transistors are connected to their respective drain regions. This technique reduces the output voltage swing due to threshold loss caused by additional MOS transistors.

LECTOR – Leakage Control Transistors: In this approach, two leakage control transistors (PMOS and NMOS) are introduced between Pull up and Pull down network [10]. They are connected such that one of the always near cut off always for any input combinations. Thus there is a sufficient resistance path between the supply rails and the ground, thereby reducing the leakage power.

3. SSVBB – Sleep Stack with variable body bias

In this section, our new low leakage power reduction technique "Sleep Stack with variable body bias" is described and compared with well known approaches like base case, sleep, sleep stack, sleepy keeper and zigzag techniques.

The main idea of variable sleepy biased keeper is to combine two well known techniques, sleep stack and keeper approach. In this approach the transistor are broken into two halves and then the sleep transistors are added in parallel to one halve of the broken transistors. The divided transistors reduce the leakage power while retaining the logic state.

During active mode, the sleep transistors are turned on. Thus the resistance to the path increases through which the delay increases substantially. The reason behind is (i) the sleep transistors added parallel is always on (ii) the resistance reduces due to parallel transistors. Therefore, we can introduce high-Vth transistors to the sleep transistors and transistors in parallel with the sleep transistor without incurring large delay overhead. As the body to source of the PMOS is on, the threshold voltage decreases, increasing the performance of the circuit. During the sleep mode, both the sleep transistors are off, thus suppressing the leakage power. PMOS is turned off, so the body to source voltage of the pull up PMOS is higher than in the active mode. Stacked transistors suppress leakage current, thus saving the state. As a result of body effect, V_{th} increases which decrease the performance.

***Sleep Stack with variable body bias SRAM cell*:**

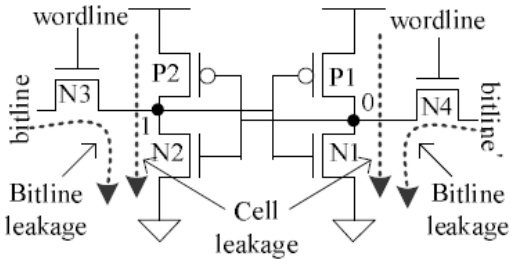

Fig.1 SRAM Cell leakage path

We design an SRAM cell based on Sleep Stack with variable body bias (SSVBB). The conventional 6T SRAM cell consists of bit line and word line pass transistors as shown in the figure. This technique can be applied to each transistor separately. Two transistors are cross coupled to access read and write operations. Bit and bit bar lines are used to transfer data during read and write operations.

There are two types of sub threshold leakage current: cell leakage and bit line leakage. Here we consider four types of variable sleepy biased keeper.

Table I: SSVBB applied to SRAM Cell

Combination	Leakage reduction
PD only	Medium
PD, WL	Medium
PU, PD	High
PU, PD, WL	High

In Table I, PD only implies that VSBK is applied to only pull down transistors of SRAM cell. This technique increases the area, due to increase in number of transistor. But maintaining the width of halved transistor greater than the maximum transistor width, there is less reduction in area.

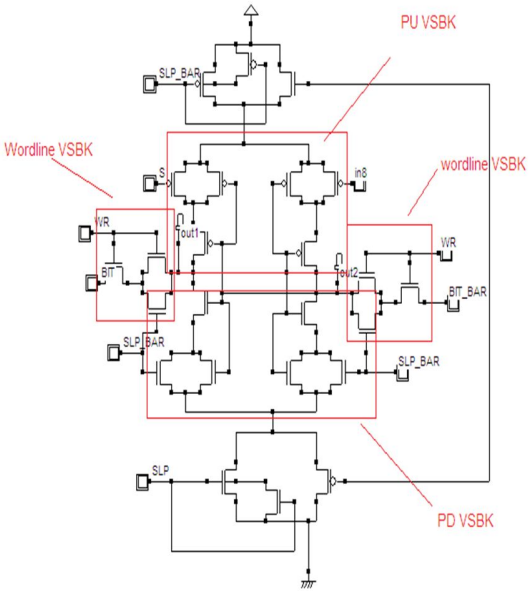

Fig.2 Variable sleepy biased keeper SRAM Cell

4. EXPERIMENTAL METHODOLOGY

We compared the proposed technique to a base case, sleep, and stack. Thus the comparison is made in terms of power, delay and power delay product. All the approaches are evaluated using low Vt transistors. The inverter uses W/L=3 for PMOS in the pull up network and W/L=1.5 for NMOS in the pull down network. All the simulations are carried down at the room temperature of 270C, VDD= 1.2v, supply voltage of 2.5V. The device model used for the simulation is BSIM model.

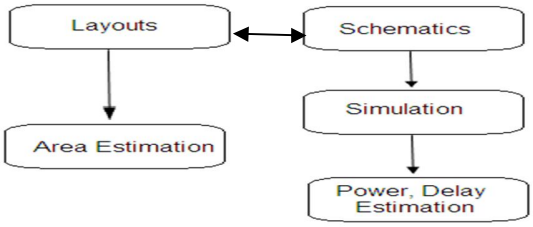

Fig. 3 Methodology

Table.2 Supply voltage applied

180nm	130nm	90 nm	65 nm	45 nm
1.8V	1.3V	1.2V	1.1V	1.0V

The Pull up device can suppress only little leakage power, while pull down device suppress majority of leakage. But leakage is not suppressed if the technique is applied to word line. SRAM Cell area can be reduced by using small sized transistors. This technique increases the area by 98% than the base case. The added sleep transistor is main reason for this area increase. Thus small sized sleep transistor has to be used which is yet great challenge.

5. RESULTS

We compare proposed technique with base case, sleepy and stack SRAM cell. We apply the technique that was discussed in Table 1.

Table.3 Technique adopted

	Technique	Power	Isub
Case 1	Low Vth	0.123mW	78 nA
Case 2	PD only	0.013µW	25nA
Case 3	PD, PU	0.012µW	43nA
Case 4	PD,WL	0.018µW	51nA
Case 5*	PU, PD, WL	0.012µW	101nA

To properly observe the technique, we compare five cases as shown in Table.3. Case 1 is the base case. In case 2, sleepy stack is applied to pull down device only. In Case 3, sleepy stack is applied to pull up and pull down device only. In Case 3, sleepy stack is applied to pull down and word line pass transistor only. The last group, sleepy stack is applied to pull up, pull down and word line only. High V_{th} is not applied, as they incur more delay than the base case.

Area

Table.4 Layout area

	Technique	Height	Width	Area
Case 1	Low Vth	7.45µ	13.1µ	97.3*e-12
Case 2	PD only	8.1µ	22.6µ	183.06*e-12
Case 3	PD , PU	10.5µ	39.75µ	417.37*e-12
Case 4	PD,WL	10.85µ	46.85µ	508.35*e-12
Case 5	PU, PD, WL	10.7µ	44.6µ	447.22*e-12

Table.4 shows the area of each technique. The area can be still reduced by using the minimum size transistors. But this in turn reduces the cell read time. As the adopted technique combines the sleepy stack and body biased, it increases the area by 98% than the base case. So the sleep transistors sizes have to be scaled properly to meet the area overhead.

Leakage power:

Leakage power is measured by changing the threshold voltage and temperature. Table 5 shows leakage power at two different temperature, 27°C and 107°C.

Table.5 Leakage power

	Technique	27°C	107°C
Case 1	Low Vth	78nW	6.6nW
Case 2	PD only	25nW	0.17µW
Case 3	PD , PU	0.068µW	0.037µW
Case 4	PD,WL	0.018µW	0.119µW
Case 5*	PU, PD, WL	0.012µW	0.037µW

Active Power:

Table.6 shows power consumption during read operation. The active power is nothing but addition of dynamic power and the leakage power. At 27°C, leakage power is 20% less than the base case for 90nm technology. But at 107°C, active power increases three times more than the base case. Thus even in active mode, power consumption is significantly affected.

Table.6 Active power consumption

	Technique	27°C	107°C
Case 1	Low Vth	7.8e-08	6.6e-09
Case 2	PD only	2.5e-08	1.7e-07
Case 3	PD , PU	6.8e-08	3.7e-08
Case 4	PD,WL	1.8e-08	1.19e-07
Case 5*	PU, PD, WL	1.2e-08	3.7e-08

6. CONCLUSIONS

In this paper we have presented a new leakage power reduction scheme “Variable sleepy biased keeper”. It provides large power saving among all the alternative schemes. There is 98% power savings compared to base case. But there is area overhead with increase of 58%.

For future work, we will explore how process variation affects leakage power using Variable sleepy biased keeper SRAM.

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